# Methodologies, Workloads, and Tools for Processing-in-Memory: Enabling the Adoption of Data-Centric Architectures

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### 1. Motivation & Problem

The increasing prevalence and growing size of data in modern applications have led to high costs for computation in traditional processor-centric computing systems. Moving large volumes of data between memory devices (e.g., DRAM) and computing elements (e.g., CPUs, GPUs) across bandwidthlimited memory channels can consume more than 60% of the total energy in modern systems [1, 2]. To mitigate these costs, the *processing-in-memory* (PIM) [1, 3–9] paradigm moves computation closer to where the data resides, reducing (and in some cases eliminating) the need to move data between memory and the processor.

There are two main approaches to PIM [4]: (1) processingnear-memory (*PnM*) [2, 10–77], where PIM logic is added to the same die as memory or to the logic layer of 3Dstacked memory [78–80]; and (2) processing-using-memory (*PuM*) [44, 81–103], which uses the operational principles of memory cells to perform computation (for example, by exploiting DRAM's analog operation to perform bulk bitwise AND, OR, and NOT logic operations [83, 84, 87, 96, 97, 99]).

Many works from academia [2, 10–12, 15–23, 25, 31, 35– 39, 48, 81-83, 85, 86, 90, 99, 104-112] and industry [34, 41–43, 50–54] have shown the benefits of PnM and PuM for a wide range of workloads from different domains. However, fully adopting PIM in commercial systems is still very challenging due to the lack of tools and system support for PIM architectures across the computer architecture stack [4], which includes: (i) workload characterization methodologies and benchmark suites targeting PIM architectures; (ii) frameworks that can facilitate the implementation of complex operations and algorithms using the underlying PIM primitives (e.g., simple PIM arithmetic operations [19], bulk bitwise Boolean in-DRAM operations [83, 84, 92]); (iii) compiler support and compiler optimizations targeting PIM architectures; (iv) operating system support for PIM-aware virtual memory, memory management, data allocation and mapping; and (v) efficient data coherence and consistency mechanisms.

Our *goal* in this work is to provide tools and system support for PnM and PuM architectures, aiming to ease the adoption of PIM in current and future systems. With this goal in mind, we address two limitations of prior works related to (*i*) identifying and characterizing workloads suitable for PnM offloading and (*ii*) enabling complex operations in PuM architectures. First, we develop a methodology, called *DAMOV*, that identifies sources of data movement bottlenecks in applications and associates such bottlenecks with PIM suitability. Second, we propose an end-to-end framework, called *SIMDRAM*, that enables the implementation of complex in-DRAM operations transparently to the programmer.

# 2. DAMOV: Identifying and Characterizing Data Movement Bottlenecks

DAMOV introduces the first rigorous methodology to characterize memory-related data movement bottlenecks in modern workloads and the first benchmark suite for data movement related studies. We develop a new methodology to correlate application characteristics with the *primary* sources of data movement bottlenecks and to determine the potential benefits of three example data movement mitigation mechanisms: (1) a deep cache hierarchy, (2) a hardware prefetcher, and (3) a general-purpose PnM architecture.

Our methodology has three steps. In *Step 1* ( $\bigcirc$  in Figure 1), we use a hardware profiling tool [113] to identify memorybound functions across applications. In *Step 2* ( $\oslash$ ), we use an architecture-independent profiling tool [114, 115] to collect metrics that provide insights about the memory access behavior of each function. In *Step 3* ( $\boxdot$ ), we collect architecture-dependent metrics and analyze the performance and energy of each function on our three data movement mitigation mechanisms. By combining the three steps, we systematically classify the leading causes of data movement bottlenecks in an application or function into different bottleneck classes.



#### Figure 1: Overview of our three-step workload characterization methodology.

Using this new methodology, we characterize 345 applications from a wide range of domains. Within these applications, we find (and fully characterize) 144 functions that are memory-bound and significantly contribute to the overall execution time. These functions are the core of our data movement benchmark suite, called DAMOV [116]. Our analyses reveal six new insights about the sources of data movement bottlenecks and their relation to PnM:

- 1. Applications with high last-level cache misses per kiloinstruction (MPKI) and low temporal locality are *DRAM bandwidth-bound*. These applications benefit from the large memory bandwidth available to the PnM system.
- Applications with low last-level cache MPKI and low temporal locality are *DRAM latency-bound*. These applications do *not* benefit from L2/L3 caches. The PnM system improves performance and energy efficiency by sending L1 misses directly to DRAM.
- 3. A second group of applications with low LLC MPKI and low temporal locality are *bottlenecked by L1/L2 cache capacity*. These applications benefit from the PnM system at low core counts. However, at high core counts (and thus larger L1/L2 cache space), the caches capture most of the data locality in these applications, decreasing the benefits the PnM system provides. We make this observation using a *new* metric that we develop, called *last-to-first miss-ratio* (*LFMR*), which we define as the ratio between the number of LLC misses and the total number of L1 cache misses. We find that this metric accurately identifies how efficient the cache hierarchy is in reducing data movement.

- 4. Applications with high temporal locality and low LLC MPKI are *bottlenecked by L3 cache contention* at high core counts. In such cases, the PnM system provides a costeffective way to alleviate cache contention over increasing the L3 cache capacity.
- 5. Applications with high temporal locality, low LLC MPKI, and low arithmetic instruction (AI) are bottlenecked by the *L1 cache capacity*. The three candidate data movement mitigation mechanisms achieve similar performance and energy consumption for these applications.
- 6. Applications with high temporal locality, low LLC MPKI, and high AI are *compute-bound*. These applications benefit from a deep cache hierarchy and hardware prefetchers, but the PnM system degrades their performance.

We publicly release our 144 representative data movement bottlenecked functions from 74 applications as the first opensource benchmark suite for data movement, called DAMOV benchmark suite, along with the complete source code for our new characterization methodology and simulator [116]. For more information on our extensive data movement bottleneck characterization and on our DAMOV benchmark suite, along with our detailed contributions (including four use cases of our benchmark suite), please refer to our full paper [5, 117].

## 3. SIMDRAM: Enabling Complex Operations using DRAM

A common approach for PuM architectures is to make use of bulk bitwise computation. Many widely-used data-intensive applications (e.g., databases, neural networks, graph analytics) heavily rely on a broad set of simple (e.g., AND, OR, XOR) and complex (e.g., equality check, multiplication, addition) bitwise operations. Ambit [83, 84, 87, 96, 97, 99], an in-DRAM PuM accelerator, proposes exploiting DRAM's analog operation to perform bulk bitwise majority-of-three (MAJ) computation, which can be manipulated to perform AND, OR, and NOT logic operations. Inspired by Ambit, many prior works have explored DRAM and emerging nonvolatile memory (NVM) [118–154] designs that are capable of performing in-memory bitwise operations [89, 92, 100, 106, 155–157]. However, a major shortcoming prevents these proposals from becoming widely applicable: they support only basic operations (e.g., Boolean operations, addition) and fall short on flexibly supporting new and more complex operations. Our goal is to design a framework that aids the adoption of processing-using-DRAM by efficiently implementing complex operations and providing the flexibility to support new desired operations.

To this end, we propose SIMDRAM, the first end-to-end framework for processing-using-DRAM. At its core, we build the SIMDRAM framework around a DRAM substrate that enables two previously-proposed techniques: (1) vertical data layout in DRAM to support bit-shift operations, and (2) majority-based logic. SIMDRAM consists of three key steps, illustrated in Figure 2, to enable a desired operation in DRAM: (1) building an efficient MAJ/NOT-based representation of the desired operation, (2) mapping the operation input and output operands to DRAM rows and to the required DRAM commands that produce the desired operation, and (3) executing the operation. We briefly describe these steps.



(b) SIMDRAM Framework: Step 3

Figure 2: Overview of the SIMDRAM framework.

The goal of the first step (① in Figure 2a) is to use logic optimization to minimize the number of DRAM row activations, and therefore the compute latency required to perform a specific operation. Accordingly, for a desired computation, the first step is to derive its *optimized* MAJ/NOT-based implementation from its AND/OR/NOT-based implementation.

The second step (2) in Figure 2a) translates the MAJ/NOTbased implementation into DRAM row activations. This step includes (1) mapping the operands to the designated rows in DRAM, and (2) defining the sequence of DRAM row activations that are required to perform the computation. SIM-DRAM chooses the operand-to-row mapping and the sequence of DRAM row activations to minimize the number of DRAM row activations required for a specific operation.

The third step () in Figure 2b) is to program the memory controller to issue the sequence of DRAM row activations to the appropriate rows in DRAM to perform the computation of the operation from start to end. To this end, SIMDRAM uses a *control unit* in the memory controller that transparently executes the sequence of DRAM row activations for each specific operation.

**System Integration.** To incorporate SIMDRAM into a real system, we address two integration challenges as part of our work: (1) managing memory with both vertical and horizontal layouts in a system, and (2) exposing SIMDRAM functionality to programmers and compilers. As part of the support for system integration, we introduce two components.

First, SIMDRAM adds a *transposition unit* in the memory controller that transforms the data layout from the conventional horizontal layout to vertical layout (and vice versa), allowing both layouts to coexist. Using the transposition unit, SIMDRAM provides the ability to store only the data that is required for in-DRAM computation in the vertical layout. SIMDRAM maintains the horizontal layout for the rest of the data and allows the CPU to read/write its operands from/to DRAM in a horizontal layout and at full bandwidth. Second, SIMDRAM extends the ISA to enable the user/compiler to communicate with the SIMDRAM control unit.

**Key Results.** We demonstrate SIMDRAM's functionality using an example set of operations including (1) *N*-input logic operations (e.g., AND/OR/XOR of more than 2 input bits); (2) relational operations (e.g., equality/inequality check, greater than, maximum, minimum); (3) arithmetic operations (e.g., addition, subtraction, multiplication, division); (4) predication (e.g., if-then-else); and (5) other complex operations such as bitcount and ReLU [158].

We compare the benefits of SIMDRAM to different stateof-the-art computing platforms (CPU, GPU, and Ambit [83, 84, 87, 96, 97, 99]). We comprehensively evaluate SIM-DRAM's reliability, area overhead, throughput, and energy efficiency. We leverage the SIMDRAM framework to accelerate seven application kernels from machine learning, databases, and image processing (VGG-13 [159], VGG-16 [159], LeNET [160], kNN [161], TPC-H [162], BitWeaving [163], brightness [164]). Using a single DRAM bank, SIMDRAM provides (1)  $2.0 \times$  the throughput and  $2.6 \times$  the energy efficiency of Ambit [83], averaged across the 16 implemented operations; and (2)  $2.5 \times$  the performance of Ambit, averaged across the seven application kernels. Compared to a CPU and a high-end GPU, SIMDRAM using 16 DRAM banks provides (1) 257× and 31× the energy efficiency, and 88× and  $5.8 \times$  the throughput of the CPU and GPU, respectively, averaged across the 16 operations; and (2)  $21 \times$  and  $2.1 \times$ the performance of the CPU and GPU, respectively, averaged across the seven application kernels. SIMDRAM incurs no additional area overhead on top of Ambit, and a total area overhead of only 0.2% in a high-end CPU. We also evaluate the reliability of SIMDRAM under different degrees of manufacturing process variation, and observe that it guarantees correct operation as the DRAM process technology node scales down to smaller sizes.

For more information on our SIMDRAM framework and our extensive evaluation results (including a comparison to an alternative framework for processing-using-cache architectures), please refer to our full paper [165, 166].

### 4. Discussion

Few prior works tackle the challenge of providing end-to-end support for PIM. We describe these works and their limitations for in-DRAM computing.

Workload Characterization and Benchmark Suites for PIM. We highlight two prior works, [167] and PrIM [41– 43] that also focus on characterizing workloads and providing benchmark suites for PIM architectures. In [167], the authors provide the first work that characterizes workloads for PIM. They analyze the benefits a PIM architecture similar to [71], where vector processing compute units are integrated into the DDRx memory modules, provides for five applications. Even though [167] has a similar goal to DAMOV, it understandably does not provide insights into modern dataintensive applications and PIM architectures as it dates from 2001. The authors of [41–43] propose PrIM, a benchmark suite of 16 workloads from different application domains (e.g., dense/sparse linear algebra, databases, data analytics, graph processing, neural networks, bioinformatics, image processing) tailored to fit the characteristics of a *real* PIM architecture (i.e., the UPMEM-based PIM system [34]). PrIM is opensource and publicly available at [168]. Unlike these prior works, DAMOV is applicable to and can be used to study other PIM architectures than processing-in/-near DRAM, including processing-in/-near cache [68, 93-95, 169-171], processingin/-near storage [40, 172–181], and processing-in/-near emerging NVMs [81, 82, 90, 91, 100, 182, 183]. This is possible since DAMOV's methodology and benchmarks are mainly concerned with broadly characterizing data movement bottlenecks in an application, independent of the underlying PIM architecture.

Frameworks for PIM. DualityCache [95] is an end-to-end framework for in-cache computing, which executes a fixed set of operations in a single-instruction multiple-thread (SIMT) manner. Employing DualityCache in DRAM is not straightforward due to the fundamental differences between in-cache computing and in-DRAM computing (e.g., the destructive behavior of DRAM operations and cost-sensitivity of DRAM chips). Two prior works, Hyper-A [184] and IMP [185], propose frameworks for in-emerging-NVM computing. Since Hyper-A and IMP target in-emerging-NVM substrates that utilize different computing paradigms (e.g., associative processing [186, 187]) or rely on particular structures of the NVM array (such as analog-to-digital/digital-to-analog converters) to perform computation, they are not applicable to an in-DRAM substrate that performs bulk bitwise operations. Olgun et al. propose the PiDRAM [188] framework, a flexible end-to-end and open-source FPGA-based framework that enables system integration studies and evaluation of in-DRAM computing techniques (e.g., in-DRAM copy and initialization [86, 98] and in-DRAM true random generation [108, 189, 190]) using real unmodified DRAM chips. PiDRAM is publicly available at [191] and can be used to prototype our SIMDRAM framework in a real system.

### 5. Conclusion & Future Work

This paper summarizes two of our recent efforts towards providing holistic system-level support for processing-in-memory (PIM) systems. We provide (i) a methodology to identify and characterize sources of data movement bottlenecks in a workload that can enable the programmer to assess whether a processing-near-memory (PnM) architecture can mitigate the identified data movement bottlenecks; (ii) the first benchmark suite (i.e., DAMOV) tailored for analyzing data movement bottlenecks and effects of near-data processing; and (iii) an end-to-end framework (i.e., SIMDRAM) that enables efficient and programmer-transparent computation of a wide range of arbitrary and complex operations by employing processingusing-memory (PuM) in DRAM. We believe that DAMOV can enable (1) simple and practical identification of PIM-suitable workloads and functions, (2) a research substrate (with our benchmark suite and simulator) for PIM-related architecture and system studies. SIMDRAM can facilitate the broader adoption of PuM architectures by more workloads and programmers. We hope that our work inspires future research on system-level solutions and tools that can aid the research, development, and implementation of PIM architectures.

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This invited extended abstract is a summary version of our two prior works DAMOV [5, 117] (published at IEEE Access 2021) and SIMDRAM [165, 166] (published at ASPLOS 2021). Presentations that describe DAMOV can be found at [192] (short talk video), [193] (long talk video), and [194] (tutorial on the DAMOV framework and benchmarks). A presentation that describes SIMDRAM can be found at [195].

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